We Claim:

1. A process for forming vias in polymers with low dielectric constants, the process comprising the steps of:

(a) providing a substrate layer;

(b) forming a lower level layer of dielectric, metal and/or circuit devices on said substrate layer;

(c) forming a seed layer on top of said lower level layer;

(d) forming a lower metal layer on said seed layer;

(e) forming one or more plated pillars having top surfaces on said lower metal layer;

(f) removing the seed player not under the lower level layer;

(g) coating said one or more plated pillars and said seed layer with a low dielectric polymer;

(h) curing said polymer;

(i) exposing said top surfaces of said plated pillars; and

(j) forming a metal layer to contact said exposed top surfaces of said plated pillars.

2. The process as recited in claim 1, wherein said coating step comprises coating with a low dielectric planarizing polymer.

3. The process as recited in claim 1, wherein said coating step comprises coating with a low dielectric, non-planarizing polymer and forming a planarizing coating over said non-planarizing polymer.

4. The process as recited in claim 1, further including the step of applying a dielectric layer to said plated pillars and bottom metal layer.

5. The process as recited in claim 4, wherein said step of applying a dielectric layer comprises applying SiO_2.

6. The process as recited in claim 4, wherein said step of applying a dielectric layer comprises applying Si_3N_4.

7. The process as recited in claim 1, wherein the step of coating comprises coating said one or more plated pillars and said lower metal layer with a silicon-based polymer.

8. The process as recited in claim 7, wherein the step of coating said one or more plated pillars and said lower metal layer comprises coating with benzocyclobutene.

9. The process as recited in claim 7, wherein the step of coating said one or more plated pillars and lower metal layer comprises coating with polynorbornene.

10. The process as recited in claim 1, wherein said step of forming said one or more plated pillars includes a step (k) of utilizing a photoresist with a re-entrant profile.

11. The process as recited in claim 10, wherein step (k) comprises utilizing a negative i-line resist.

12. The process as recited in claim 10, wherein step (k) comprises utilizing a NH_3 image reversal of a positive photoresist.

13. A process for forming vias in polymers with low dielectric constants, the process comprising the steps of:

(a) providing a substrate layer;

(b) forming a lower level layer of dielectric, metal and/or circuit device on said substrate;

(c) forming a bottom metal layer on said lower level layer;

(d) forming one or more pillars from a photoresist on said lower metal layer;

(e) coating said one or more pillars with a polymer;

(f) curing said polymer;

(g) etching back said polymer to expose said photoresist pillars

(h) removing said one or more photoresist pillars to form vias; and

(i) forming a metal layer to contact said bottom metal layer on top of said polymer coating.

14. The process as recited in claim 13, further including the steps of:

(j) forming a dielectric on top of said bottom metal layer and said lower level layer before said coating step; and

(k) removing said dielectric layer from said bottom metal layer before said metal layer is formed on top of said polymer coating.

15. The process as recited in claim 14, wherein said step of forming a dielectric comprises forming a SiO_2 layer.

16. The process as recited in claim 14, wherein said step of forming a dielectric comprises forming a Si_3N_4 layer.

17. The process as recited in claim 13, wherein said coating step comprises coating with a low dielectric planarizing polymer.

18. The process as recited in claim 13, wherein said coating step comprises coating with a low dielectric, non-planarizing polymer and forming a planarizing coating over said non-planarizing polymer.

19. The process as recited in claim 13, wherein the step of coating comprises coating said one or more photoresist pillars with a silicon-based polymer.

20. The process as recited in claim 19, wherein the step of coating said one or more photoresist pillars comprises coating with benzocyclobutene.

21. The process as recited in claim 19, wherein the step of coating said one or more photoresist pillars comprises coating with polynorbornene.

22. The process as recited in claim 13 wherein the step of forming one or more pillars includes a step (l) of utilizing a photoresist with a re-entrant profile.

23. The process as recited in claim 22, wherein step (l) comprises utilizing a negative i-line resist.

24. The process as recited in claim 22, wherein step (l) comprises utilizing a NH_3 image reversal of a positive photoresist.